a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

REMARKS

By this amendment, claims 19 and 38 are amended, and claims 43-47 have been added. No new matter has been added. Accordingly, Claims 19-47 are pending in this application and are submitted for consideration.

Claims 22-37 are allowed.

Claims 20-21 and 39-42 were found to contain allowable subject matter but were objected to for being based upon a rejected base claim. Claims 20-21 and 39-42 would be allowed if rewritten into independent form. Since all outstanding rejections are addressed herein, the Applicant requests that claims 20-21 and 39-42 be allowed.

In the Final Office Action dated May 3, 2002, claims 19 and 38 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,920,208 to Park. Claim 19 was also rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,929,655 to Roe. The Applicant submits that claims 19 and 38, as submitted herein, recite subject matter not shown or described by the cited prior art.

Claim 19 defines an input buffer circuit, which includes a differential amplifier circuit, first and second circuits, and a control circuit. The differential amplifier circuit is disposed between a first power supply and a second power supply and is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is coupled to the differential amplifier circuit and is for receiving the amplified signal from the

differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply and is for receiving the first input signal. The control circuit is for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal. The control circuit isolates a disabled one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

Claim 38 defines an input buffer circuit, which includes a differential amplifier circuit, first and second circuits, and a control circuit. The differential amplifier circuit is for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. The first circuit is disposed between a first power supply and a second power supply and is for receiving the amplified signal from the differential amplifier circuit. The second circuit is disposed between the first power supply and the second power supply and is for receiving the first input signal. The control circuit is coupled to the differential amplifier circuit and the first and second circuits and is for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal. The control circuit isolates a disabled one of the first circuit and the second circuit from the first power supply or the second power supply.

Regarding Park, it was asserted in the Office Action that transistors 20-24 and 30 of Fig. 1 of Park correspond to the differential circuit and that transistors 25-30 correspond to the second circuit, of the present invention. However, in contrast to the claimed invention, the circuit comprising the transistors 20-24 and the circuit comprising transistors 25-29 are enabled at the same time by the transistor 30. See column 5,

lines 4-51 of Park. In contrast, according to claims 19 and 38, only one of the differential amplifier circuit and the second circuit is enabled (or one of the disabled differential amplifier circuit and the second circuit is isolated from the first power supply or the second power supply). Thus, Park fails to show or describe each and every element of claims 19 and 38.

Regarding Roe, it was asserted in the Office Action that the output buffer 202 of Roe corresponds to the second circuit of claim 19. However, the Applicant submits that if there is a corresponding circuit, it would have to be input buffer 206 because it receives a first signal. Therefore, the input buffer 206 is addressed in the following remarks.

In the Office Action, it was asserted that the differential input buffer 212 of Roe corresponds to a differential amplifier circuit of claim 19, and that the input buffer 206 corresponds to the second circuit. However, since the input buffer comprises a NOR gate 372 and an inverter 374, as shown in Fig. 4 of Roe, the input buffer 206 is not controlled or configured to be isolated from the first power supply or the second power supply, as required by claim 19.

Furthermore, Roe's differential input buffer 212 has two outputs, and Roe's input buffer 206 has one output. Accordingly, the Applicant submits that it is necessary to separately provide first signal lines for the two outputs of the buffer 212 and a second signal line for the one output of the input buffer 206. In contrast, the second circuit of claim 19 generates an output signal and provides it to a first circuit, which receives an amplified signal from the differential amplifier circuit. That is, an output signal line to the first circuit is shared by the differential amplifier circuit and the second circuit, thereby

reducing a circuit area. Thus, the Applicant submits that Roe fails to show each and every element of claim 19.

The Applicant submits that new claims 43-47 recite subject matter not shown or described by the cited prior art. In particular, new claim 43 recites that a control circuit selectively enables one of the differential amplifier circuit and the second circuit in accordance with a control signal. New claim 44 recites that a control circuit selectively isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply. New claim 45 recites that a second circuit generates an output signal to the first circuit, which is supported at page 6, lines 32 to page 7, line 2 of the present specification. New claim 46 is a modified version of claim 43 and recites that the differential amplifier circuit generates a single amplified signal and the second circuit generates a single output signal. New claim 47 is a modified version of claim 44 and add the word "single" like new claim 46.

In view of the above remarks, the Applicant respectfully submits that each of claims 19-47 recite subject matter which is neither disclosed nor suggested in the cited prior art. The Applicant submits that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. The Applicant therefore requests that each of 19-47 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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MARKED UP COPY OF AMENDED CLAIMS

19. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, [connected] coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit isolates a disabled one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

38. (Once Amended) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit, [connected] coupled to the differential amplifier circuit and the first and s cond circuits, for selectively enabling the differential amplifier circuit and [the first and second circuits] one of the first circuit and the second circuit in accordance with a control signal, wherein the control circuit isolates a disabled one of the first circuit and the second circuit from the first power supply or the second power supply.